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(54) Logic circuit.

(57) A logic circuit is presented comprising a plurality of registers 30, 39; each register 30 having first register latches 31, 41 for clocking data into the register 30 in response to a first clock signal 37 and second register latches for clocking data out of the register in response to a second clock signal 38, and combinatorial logic comprising address logic 4 for addressing data to a register and first suppression logic 33 for inhibiting the first clock signal input to the register in responsive to the address logic, wherein the logic circuit further comprises second suppression logic 34, 35 for inhibiting the second clock signal input to the register in collective response to the address logic and the first clock signal.

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LOGIC CIRCUIT

The present invention relates to a logic circuit, more specifically, to logic circuit including a clocking arrangement for clocking data through multiple bit registers in the circuit.

Synchronous Complementary Metal Oxide Semiconductor (CMOS) logic circuits are commonly designed according to a Level Sensitive Scan Design (LSSD) technique. These LSSD circuits are responsive to a combination of a C clock signal and a B clock signal. The C clock signal and the B clock signal are non-overlapping. More specifically, although they are of the same frequency, it is a requirement of LSSD that active periods of the two clock signals do not coincide. A register in the logic circuit, designed according to an LSSD technique, consists of an array of Shift Register Latches (SRLs). An SRL consists of a first latch responsive to the C clock signal and a second latch responsive to the B clock signal. When the C clock signal is true, an input data bit is stored in the first latch. When the B clock signal is true, the input data bit is passed from the first latch and stored in the second latch. For the purpose of explanation, and to highlight aspects of the present invention, a process by which a latch responds to a clock signal by storing a data bit shall hereinafter be referred to as clocking.

Many synchronous logic circuits include a large number of multiple bit registers and may therefore contain thousands of SRLs. Power consumption problems can arise if such a logic circuit is manufactured by integrating CMOS devices on a silicon substrate. Logic gates consisting of CMOS devices consume most electrical power whilst in transience between logical states. This power is dissipated as heat. Therefore, the power consumed by many thousands of CMOS SRLs, switching on every clock cycle, makes a significant contribution to heat dissipated by a logic circuit. Such heat dissipation can restrict the choice of packaging material for encapsulating the logic circuit to those material with suitable heatsinking properties, which may not be the cheapest materials available. Therefore, since there is a demand for denser device integration and faster clock rates, to increase on-chip processing power, the need has arisen to examine methods for reducing power consumption associated with CMOS device technology.

Some synchronous logic circuits include registers for storing dependent data groups as "set-up" parameters. Such data groups are modified infrequently during normal operation of the logic circuit. When such a data group changes, an address word, associated with the data group, can be generated by combinatorial logic in the logic circuit. The address word can be further decoded by the combinatorial logic to produce a true state in an I/O address line which is otherwise held false. In a similar fashion, other I/O address lines can be associated with other data groups stored in other registers in the synchronous logic circuit. In one such known synchronous logic circuit design, a separate suppression gate corresponds to every register storing a dependent data group. The suppression gate prevents the C clock signal from clocking the first latches of a register unless an associated I/O address line is true. Such a function is referred to in the art as a gating function. This arrangement has the advantage that the use of C clock suppression can reduce the complexity of addressing logic and therefore the cost of combinatorial logic in the logic circuit. Furthermore, C clock suppression also provides some reduction in power consumed by a logic circuit. However, while the C clock signal to a particular register may be inhibited, because a corresponding I/O address line is false, the B clock signal continues to clock the second latches in the register thereby causing unnecessary power consumption.

The aim of the present invention, therefore, is to provide a clock architecture for minimising the power consumed by a synchronous CMOS logic circuit.

According to the present invention there is now proposed a logic circuit comprising a plurality of registers; each register having first register latches for clocking data into the register in response to a first clock signal and second register latches for clocking data out of the register in response to a second clock signal, and combinatorial logic comprising address logic for addressing data to a register and first suppression logic for inhibiting the first clock signal input to the register in response to the address logic, wherein the logic circuit further comprises second suppression logic for inhibiting the second clock signal input to the register in collective response to the address logic and the first clock signal.

A logic circuit in accordance with the present invention has the advantage of providing a second gating function, applicable to the second clock signal yet responsive to the first clock signal, by which means data is now only admitted to any register when data stored therein is to change. The number of clock transitions undergone by second latches in the logic circuit can now be reduced. Since the first clock signal input to such a register may be subject to a first gating function, a mechanism is provided for further reducing power con-

sumed by a CMOS logic circuit.

A particular embodiment of the present invention, and aspects of logic circuitry to which the invention relates will now be described with reference to the following diagrams in which:

Figure 1 is a block diagram of a general logic circuit having an LSSD architecture.

Figure 2 is a block diagram of an LSSD register structure for the logic circuit.

Figure 3 is a block diagram of another LSSD register structure for the logic circuit.

Figure 4 illustrates a timing relationship between the C clock signal and the B clock signal associated with the LSSD architecture.

The present invention is broadly applicable to processing logic implemented by Very Large Scale Integration (VLSI) of (e.g CMOS devices) on a silicon substrate. The general logic circuit shown in Figure 1 is symbolic of such processing logic. Therefore, for background information, this general logic circuit, which may include an example of logic in accordance with the present invention, will now be described. The general logic circuit consists of a multiple bit register block 3 for data storage and a combinatorial logic network 4 for data processing. The multiple bit register block consists of separate registers for storing feedback data 1. The feedback data is passed through the multiple bit LSSD register block to the combinatorial logic in response to a non-overlapping clock stimulus 22, 23 produced by a clock generator 5. As a result of such stimulus and additional input data 6, both the feedback data and data output 8 from the logic circuit can be refreshed.

An LSSD register structure arranged in accordance with the present invention will now be described with reference to Figure 2. This register structure consists of separate registers for storing data groups associated with the logic circuit. For instance, register 30 is used to store data group A. Data bit a1 of data group A is stored in SRL latch 36. First latch 31 of SRL array 36 loads data bit a1 in response to a true state in the C clock signal 37 occurring during a period for which address line Ca is also true. AND gate 33 prevents the C clock signal from clocking the first latches in the register when address line Ca is false. The register also includes a control latch 34 into which the state of the address line Ca is loaded in response to a true state in the C clock signal. Second latch 32 of SRL array 36 loads data bit a1 in response to a true state in the B clock signal 38 occurring during a period for which delayed address line C'a is also true. The state of delayed address line C'a is specified by the contents of the control latch. AND gate 35 prevents the B clock signal from clocking the second latches in the register when delayed address line C'a is false. More specifically, during a true state in the B clock signal, the state of the delayed address line C'a is the same as that of the address line Ca during the immediately preceding true state of the C clock signal. A "look ahead" clock structure is therefore provided whereby the B clock signal only clocks the register in response to the C clock signal previously clocking the register which, in turn, is made possible by switching address line Ca to a true state.

Referring to Figure 2, it can be seen that this "look ahead" clock structure can be implemented in as many registers in the logic circuit as necessary. For instance, in Figure 2, another register 39 for storing data group B has a similar topology to register 30 for storing data group A. However, in the case of data group B, the C and B clock signals clock register 39 subject to the status of address line Cb. Therefore, by way of the present invention, such address lines can now select which registers the B clock signal is applied to, in addition to selecting which registers the C clock signal is applied to. It follows that this example of the "look ahead" clock structure can significantly reduce the number of clock transitions to which registers in the logic circuit are subjected. The degree of power reduction depends on the number of B clock cycles for which the address lines are true. If the address lines are true more often than they are false, the degree of power reduction will be accordingly small. It follows therefore, that the present invention is particularly applicable to those logic circuits comprising a large number of registers for storing "set-up" parameters which are changed infrequently during normal operation.

By way of another example of the present invention, another LSSD register structure is shown in Figure 3. This register structure has a similar "look ahead" clock function to that described in the preceding paragraphs. However in this case an alternative "look ahead" clock structure is employed. This alternative "look ahead" clock structure will now be described with reference to Figure 3 in which register 50 is for storing the data group A as used in the description of the previous example. Data bit a1 is stored in SRL 54. First latch 55 of SRL 54 loads data bit a1 in response to a true state in the C clock signal occuring during a period for which both address line Ca and I/O write line W 53 are true. AND gate 56 prevents the C clock signal from clocking the first latches in register 50 except when I/O write line W and address line Ca are true simultaneously. Second latch 57 of SRL array 54 loads data bit a1 in response to a true state in the B clock signal occurring during a period for which delayed I/O write line W′ is also true. The state of delayed I/O write line W′ is specified by the contents an I/O write latch 52 which loads the state of the I/O write line W in

response to a true state in the C clock signal. AND gate 58 prevents the B clock signal from clocking the second latches in register 50 when the delayed I/O write bit W′ is false. AND gate 58 and the I/O write latch implement a "look ahead" clock function which can not only prevent the B clock signal from clocking register 50, but also from clocking register 51, which is for storing data group B, and into which data group B can be loaded in only when address line Cb is true during a true state in the C clock signal. In this structure, a "look ahead" clock function can be implemented in as many registers in the logic circuit as necessary via the addition of a single control latch, a single AND gate, and a single additional I/O write bit. By contrast, in the example of the present invention described in the preceding paragraphs, each register was assigned individual B clock suppression logic consisting of separate latch and AND gate. The example of the present invention described in this paragraph is therefore a less complicated implementation. The degree of power reduction provided by this structure depends on the number of B clock cycles for which the I/O write bit is true. The I/O write bit is true when signifying a change in data stored in the registers. If the I/O write bit is true more often than it is false, the degree of power reduction will be accordingly small. However, as stated in the preceding paragraphs, such circumstances are unlikely to arise in logic circuits having a large number of registers for storing "set-up" parameters which are changed infrequently during normal operation.

The clock signal timing diagram shown in Figure 4 illustrates an example phase relationship between the C clock signal 71 and the B clock signal 70 for clocking the register structures shown in Figure 2 and Figure 3. Logic circuits produced by interconnecting CMOS devices contain parasitic impedances which give rise to signal delays. Such delays can cause spurious signals to propagate through the logic circuit. It is therefore necessary to define a "settling" interval t1 after each true state 72 of one clock signal during which the other clock signal is held false.

For the purpose of illustrating the present invention, the register structures described hereinbefore are composed of LSSD register latches; each latch being fabricated by the very large scale integration of CMOS devices. It will be appreciated, however, that the present invention is not limited in application to such logic circuits. Clearly, the present invention is applicable to any logic circuit in which data is processed in response to a set of non overlapping clock signals and from which power is dissipated during periods of transience in such clock signals.

Claims

1. A logic circuit comprising a plurality of registers (30,39); each register (30) having first register latches (31,41) for clocking data into the register (30) in response to a first clock signal (37) and second register latches for clocking data out of the register in response to a second clock signal (38), and combinatorial logic comprising address logic (4) for addressing data to a register and first suppression logic (33) for inhibiting the first clock signal input to the register in response to the address logic, wherein the logic circuit further comprises second suppression logic (34,35) for inhibiting the second clock signal input to the register in collective response to the address logic and the first clock signal.

2. A logic circuit as claimed in claim 1 wherein the second suppression logic comprises a plurality of control latches (34,40); each latch corresponding to a register for responding to the first clock signal, by storing an address bit for addressing data to the register; the address bit being generated by the address logic.

3. A logic circuit as claimed in claim 2 wherein the second suppression logic comprises a plurality of control gates (35,42); each control gate corresponding to a register for admitting the second clock signal to the register subject to a corresponding control latch containing a particular bit value.

4. A logic circuit as claimed in claim 1 wherein the second suppression logic comprises one control latch (52) for responding to the first clock signal by storing a write bit (53) generated by the address logic.

5. A logic circuit as claimed in claim 4 wherein the second suppression logic comprises one control gate (58) for admitting the second clock signal to the registers subject to the control latch containing a particular bit value.

6. In a logic circuit, comprising a plurality of registers; each register having first register latches for clocking data into the register in response to a first clock signal and second register latches for clocking data out of the register in response to a second clock signal, and first suppression logic for inhibiting the first clock signal input to the register in response to address logic, a method for inhibiting the second clock signal comprising the steps of:

storing address bits in a plurality of control latches in response to the first clock signal; each latch corresponding to a register storing an address bit for addressing data to the register; the address bit being generated by the address logic,

gating the second clock signal by gating means comprising a plurality of control gates; each control gate corresponding to a register for admitting the

second clock signal to the register subject to a corresponding control latch containing a particular bit value;

7. In a logic circuit, comprising a plurality of registers; each register having first register latches for clocking data into the register in response to a first clock signal and second register latches for clocking data out of the register in response to a second clock signal, and first suppression logic for inhibiting the first clock signal input to the register in response to address logic, a method for inhibiting the second clock signal comprising the steps of:

storing a write bit in one control latch in response to the first clock signal; the write bit being generated by the address logic.

gating the second clock signal by gating means comprising a control gate for admitting the second clock signal to the registers subject to the control latch containing a particular bit value.

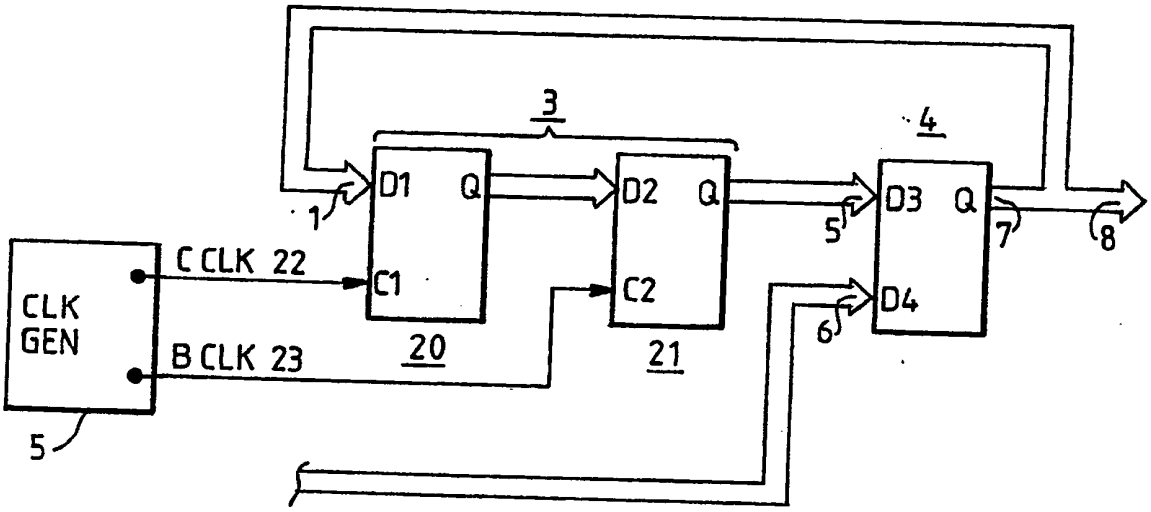
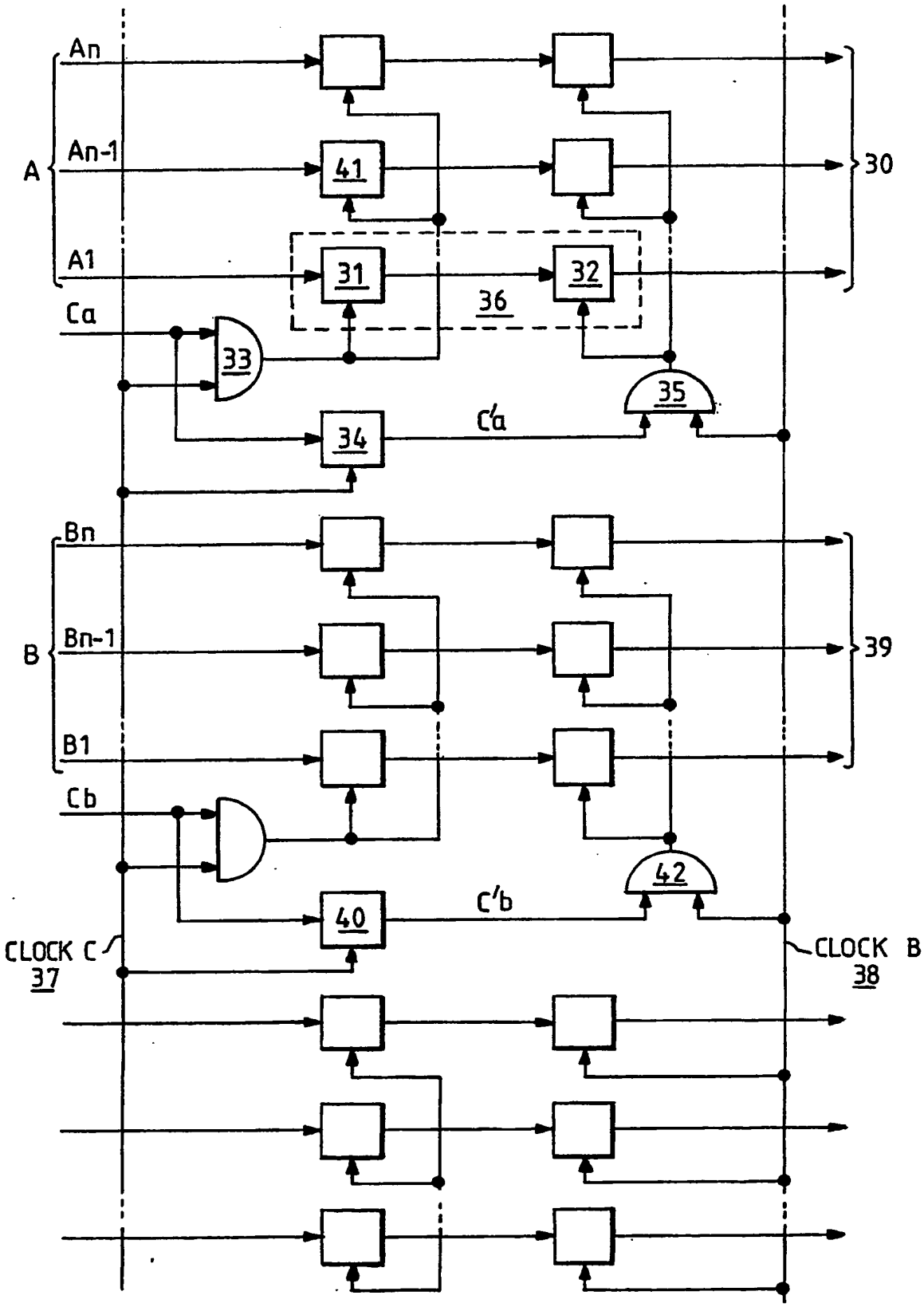


FIG. 1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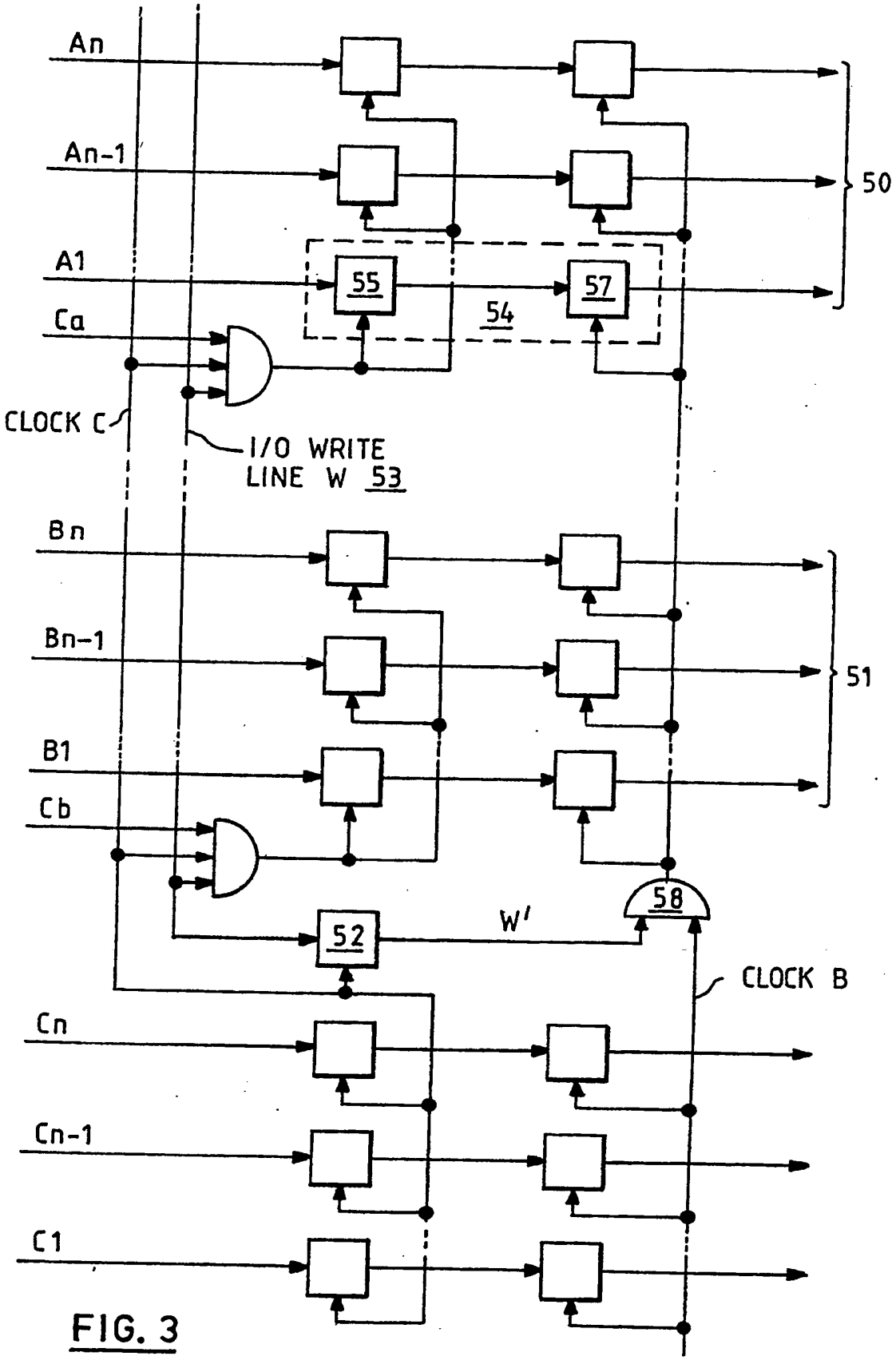
An-1
A
A1
30
41
31
32
36
Ca
33
35
34
C'a
Bn
Bn-1
B
B1
39
Cb
42
40
C'b
CLOCK C
37
CLOCK B
38

FIG. 2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55
57
54
50
Bn
Bn-1
B1
Cb
51
52
W'
58
CLOCK B
Cn
Cn-1
C1

FIG. 3

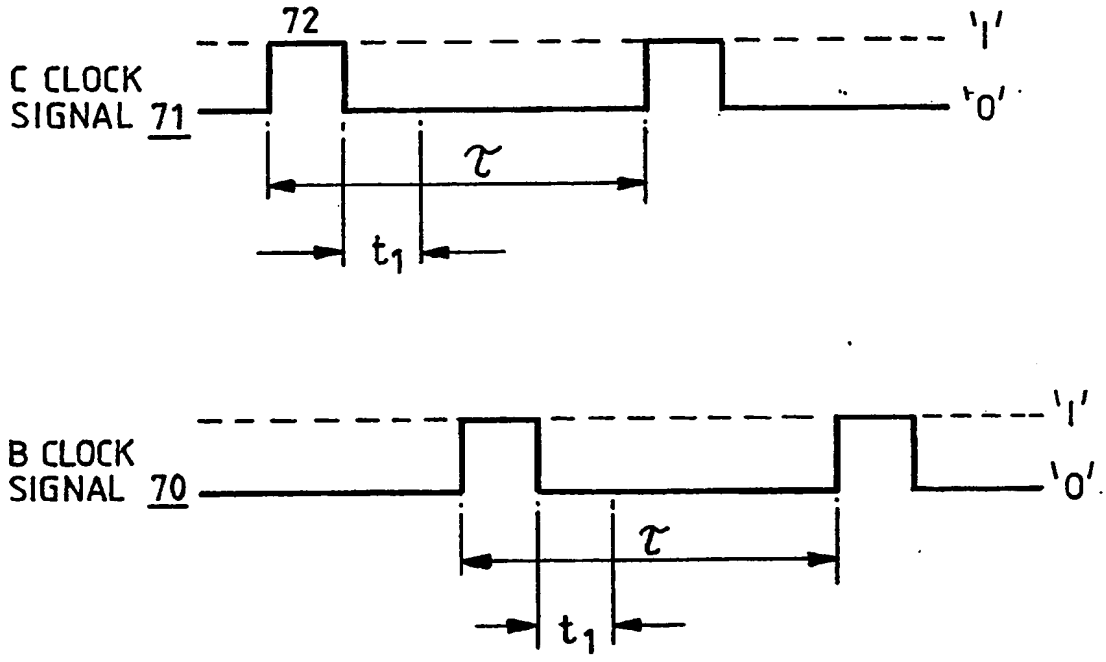

FIG 4

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EUROPEAN SEARCH REPORT

Application Number

EP 89 31 2532

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 18, no. 11, April 1976, pages 3711-3712, New York, US; T.J. BLAZEJEWSKI et al.: "Secondary path requiring only one additional connection" * Whole document *	1	G 01 R 31/318 G 11 C 19/00
Y	IDEM	2,3,6	
Y	EP-A-0 289 158 (TANDEM)(02-11-1988) * Abstract; column 5, lines 2-25; column 6, line 47 - column 7, line 9; figure 6 *	2,3,6	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 30, no. 3, August 1987, pages 1327-1330, Armonk, New York, US; "Reading L2 and gated B clock shift register latches using a bring-up tool to scan out the values while preserving machine state" * Whole document *	1-7	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	PROCEEDINGS INTERNATIONAL TEST CONFERENCE 1984, 1984, pages 338-347, IEEE, New York, US; H.H. BUTT et al.: "Impact of mixed-mode self-test on life cycle cost of VLSI based designs" * Page 340, paragraph "MMST-I"; table 1; figures 3-4 *	1-7	G 01 R G 06 F G 11 C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	06-07-1990	SARASUA GARCIA L.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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